AURORA'S ENGINEERING COLLEGE

BHONGIR, NALGONDA DIST. – 508116.

Lab manual of

e-CAD & VLSI Laboratory

4ECE, 1st Semester, 2014-15

(As per 2009 Regulation)

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

PREFACE

ECAD environments provide the tools for generating a physical representation of the integrated circuit from a high-level description. Traditionally, the designer starts with a schematic representation at a transistor or logical level, but due to the huge complexity of modern integrated circuits the trend is to use higher ones, such as in *Hardware Description Languages (HDLs).*

The physical representation specifies how a particular part of the integrated circuit will be constructed. At the lowest level it is the photo-mask data necessary to perform the several processing steps. To simplify, a model based on material layers is used. These layers (forming the layout) are afterwards translated into photo-masks. The poly layer, for example, specifies where the first layer of polysilicon will be deposited to form the gate of a transistor or a local interconnection. Sometimes these layers do not relate to a specific material but to material modifications as in implantation/diffusion steps.

The layout design rules are the link between the circuit designer and the technology constraints which the former must fulfill so that the fabricated integrated circuits may achieve a sufficiently high yield. ECAD tools always provide a *Design Rule Checker (DRC)* to inform the designer whether they are being correctly considered or not. Aside those rules the circuit designer is usually not concerned with technology related aspects, as in the ECAD environment these are encapsulated in simple parameters like the sheet resistance of one layer, or capacitance per unit area between two layers. This makes the actual thickness of the layers of little importance. For the active devices, circuit simulator models as the *SPICE* Level 3 model are employed. They must be calibrated for a given technology and afterwards need only relatively few layout-dependent parameters. For integrated circuits with millions of transistors, similarly to what happens in its description, a circuit-level simulation is not practical and ECAD tools provide logic-level and register level simulators as well. A very important aspect in future integrated circuit design is testability. ECAD frameworks include also tools to support the design for testability.

LAB CODE

1. Students should report to the concerned labs as per the timetable schedule.

2. Students who turn up late to the labs will in no case be permitted to perform the experiment scheduled for the day.

3. After completion of the experiment, certification of the concerned staff in-charge in the observation book is necessary.

4. Students should bring a notebook of about 100 pages and should enter the readings/ observations into the notebook while performing the experiment.

5. The record of observations along with the detailed experimental procedure of the experiment performed in the immediate last session should be submitted and certified by the staff member in-charge.

6. Not more than three students in a group are permitted to perform the experiment on a setup.

7. The group-wise division made in the beginning should be adhered to, and no mix up of student among different groups will be permitted later.

8. The components required pertaining to the experiment should be collected from stores in-charge after duly filling in the requisition form.

9. When the experiment is completed, students should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.

10. Any damage of the equipment or burnout of components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year.

11. Students should be present in the labs for the total scheduled duration.

12. Students are required to prepare thoroughly to perform the experiment before coming to Laboratory.

13. Procedure sheets/data sheets provided to the students' groups should be maintained neatly and to be returned after the experiment.

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